REMARKS

The Applicant's representative has carefully reviewed and considered the Office Action mailed on August 14, 2001, including the references cited therewith. In this timely-filed Response, no claims are amended, no claims are canceled, and no claims have been added. Accordingly, claims 11-21 and 59-71 are pending in this application.

Attention is respectfully directed to the fact that, although an indication was made as to the rejection of claim 71 on form PTO-326 in the Office Action, no reason for such rejection was given in the body of the Action. In order for the Applicant to properly address the concerns of the Examiner regarding this claim, specific reasons for its rejection are requested if claims 11-21 and 59-71 are not found to be in condition for allowance after considering the following discussion.

§102 Rejection of the Claims

Claims 11-21 and 59-71 were rejected under 35 U.S.C. § 102(b) as being anticipated by Manning (U.S. Patent No. 5,610,864). However, the M.P.E.P. requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131. Thus, the Applicant asserts that the Office Action has failed to show that Manning discusses the identical invention claimed in the instant application, and respectfully traverses this rejection.

More particularly, the Applicant was unable to find where Manning discusses subject matter involving "switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected," as claimed in the instant application. Perhaps the "patternless addressing scheme", including "random column address access" of the instant application has been interpreted to be disclosed by col. 5, lines 43-50 of Manning? As will be shown below, such is not the case.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in another Office Action mailed to the Applicant on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If

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Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and *pipelined* modes of operation, as claimed in claims 17, 59-61, 64, and 70-71? The Applicant also respectfully draws attention to numerous statements in the instant Office Action which assert that Manning discloses a "control circuit for selecting between an unpatterned pipeline and a patterned burst data pattern", or similar statements (see Office Action § 3, regarding claims 59-61, 64, and 70-71). The Applicant's representative was unable to find any portion of Manning to support the idea that Manning includes such circuitry, and requests that such support for this proposition be designated with more specificity.

Second, the Office Action has failed to produce a *prima facie* case of anticipation. The only references offered to support the assertion that Manning "discloses the invention as claimed" with respect to claim 1 are: Fig.1, Ref. 38; col. 5, lines 43-50; col. 6, lines 14-32; and col 7, lines 43-54). Fig. 1, Ref. 38 is a block labeled generic DRAM control logic, with no indication whatsoever regarding exactly which modes may be operative, or how they may be selected. Col. 5, lines 43-50 discuss the possibility of using a pipelined architecture as an *alternative* to burst operation, but not as enabling switching between pipeline or burst operations, on-the-fly, within the *same* memory, as disclosed and claimed by the Applicant. Col. 6, lines 14-32 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Again, Manning gives no support whatever to the idea that a pipelined mode of operation is the same as a fast page mode. Thus, Manning never discusses the ability to *select* between burst and pipelined modes of operation, or patternless and patterned addressing schemes, as claimed by the Applicant in independent claim 11, as well as in independent claims 59-62, 65, 68 and 70, and all of the claims which depend from them.

The MPEP requires that "[d]uring patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.'" See M.P.E.P. § 2111. The Applicant respectfully submits that the interpretation of the Office is neither reasonable nor consistent with the instant specification, which describes how to switch depending on which of the patternless or patterned addressing schemes are selected. It is unreasonable to interpret the mere mention of the existence of a pipelined architecture by Manning as enabling switching

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between patternless and patterned addressing schemes, as disclosed and claimed in the instant application.

In short, what Manning discusses is not identical to the subject matter of Applicant's invention, and therefore, the rejection is improper, and should be withdrawn. Reconsideration and allowance of claims 11-21 and 59-71 is thus respectfully requested.

CONCLUSION

The Applicant's representative has reviewed the other art made of record by the Office, but believes that the cited art is more pertinent to the instant application. Thus, the Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly solicited. The Examiner is invited to telephone Applicant's attorney at (612) 371-2129 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2129

Date 10/30/2001 By _____
Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 30 day of October, 2001.

Tina Pugh
Name

Signature

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